

UNITED STATES PATENT APPLICATION

For

ZEOLITE – CARBON DOPED OXIDE COMPOSITE LOW K DIELECTRIC

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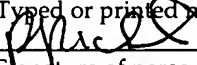
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ZEOLITE – CARBON DOPED OXIDE COMPOSITE LOW K DIELECTRIC

FIELD

[0001] This invention relates to the field of fabricating semiconductor devices and, in particular, to composite low k dielectrics.

BACKGROUND

[0002] Modern integrated circuits generally contain several layers of interconnect structures fabricated above a substrate. The substrate may have active devices and/or conductors that are connected by the interconnect structure.

[0003] Interconnect structures, typically comprising trenches and vias, are usually fabricated in, or on, an interlayer dielectric (ILD). It is generally accepted that, the dielectric material in each ILD should have a low dielectric constant (k) to obtain low capacitance between conductors. Decreasing this capacitance between conductors, by using a low dielectric constant (k), results in several advantages. For instance, it provides reduced RC delay, reduced power dissipation, and reduced cross-talk between the metal lines.

[0004] Materials commonly used to achieve low k dielectrics/films are carbon doped oxides (CDOs) or amorphous CDOs. CDOs tend to have a k value less than 3.5, but suffer from weak mechanical properties. These weak mechanical properties often result in cracking of the CDO during high stress processing and packaging steps.

[0005] Another material that may be potentially used for ILDs is zeolite or silica zeolite. Zeolite material is advantageous in that they have high porosity and a relatively uniform pore distribution. Zeolite material also is known to have good mechanical

strength. Furthermore, zeolite films have dielectric constants in the range of 2.7 and smaller. Yet, zeolite is a crystalline structure, which makes forming a uniform film extremely difficult.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention is illustrated by way of example and not intended to be limited by the figures of the accompanying drawings.

[0007] Figure 1 illustrates a solution with zeolite particles dispersed in the solvent.

[0008] Figure 2 is a cross-sectional elevation view of an underlying layer with a conductor and an etch stop disposed on the underlying layer.

[0009] Figure 3 is a cross-sectional elevation view of the solution from Figure 1 after it has been deposited on the underlying layer from Figure 2 and at least some of the solvent has been removed to form a zeolite film.

[0010] Figure 4 is a cross-sectional elevation view of Figure 3 after a carbon doped oxide precursor has been deposited in the porous zeolite film to form a zeolite - CDO film.

[0011] Figure 5 is a cross-sectional elevation view of Figure 4 after the zeolite - CDO film has been calcinated.

[0012] Figure 6 is a cross-sectional elevation view of Figure 5 after a via opening and a trench have been etched.

[0013] Figure 7 is a cross-sectional elevation view of Figure 6 after a barrier layer has been deposited on the surfaces of the zeolite - CDO film and a conductive material has been formed in the via opening and the trench.

[0014] DETAILED DESCRIPTION

[0015] In the following description, numerous specific details are set forth such as examples of specific solvents, deposition methods, carbon doped oxides, etc. in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well known methods and materials, such as spin-coating, dip-coating, and zeolite nano-particle preparation have not been described in detail in order to avoid unnecessarily obscuring the present invention.

[0016] The method and interconnect structure described herein are for forming interlayer dielectrics (ILDs) from a zeolite – carbon doped oxide (CDO) composite. A composite may be any combination of two or more materials, such as a carbon doped oxide and zeolite, whether actual bonds are present or not. A composite may also be a material formed from a combination of materials which differ in composition or form and retain their identities and properties. A composite may also include a nano-composite, where the zeolite particles are nano sized.

[0017] Referring to **Figure 1**, a solvent – zeolite solution 115 is depicted. Solvent – zeolite solution 115 may be any suspension, mixture, solution, or colloid comprising solvent 105 and zeolite particles 110. Zeolite particles 110 are dispersed in solvent 105. Solvent 105 may be any low molecular solvent, such as water, or solvent 105 may be any organic oligomer, such as polyethylene glycol, poly styrene, poly (Methacrylates), Poly (acrylate), poly ethylene oxide, or any other organic oligomer. Zeolite particles 110 may be dispersed in solvent 105 by adding them to solvent 105. Furthermore, zeolite particles 110 may be may be dispersed in solvent 105 by stirring both zeolite particles 110 and

solvent 105. For example, zeolite particles 110 may be dispersed/stirred into solvent 105 by putting the solution in a centrifuge and spinning solvent 105 until zeolite particles 110 are suspended in solvent – zeolite solution 115.

[0018] Zeolite particles 105 may be any size particles including nano-sized particles. Nano-sized zeolite particles may be obtained by spinning a zeolite – solvent solution at low speeds to separate out the large zeolite particles. Furthermore, the amount of zeolite particles 110 may be varied to obtain different zeolite concentration in the solvent - zeolite solution 115, as well as the properties of the final zeolite – carbon doped oxide composite, which is discussed later in reference to **Figures 4 – 7**.

[0019] Turning to **Figure 2**, and underlying layer 205 is depicted, which often is comprised of several active devices and/or a layer with conductors exposed. Underlying layer 205 may be a semiconductor wafer including device regions; other structures such as gates, local interconnects, metal layers, or other active/passive device structures or layers.

[0020] In **Figure 2**, underlying layer 205 has underlying conductor 210. Underlying conductor 210 may be copper or copper alloy, as well as some other conductive material such as gold. Underlying layer 205 may also be a carbon doped oxide – zeolite composite dielectric in accordance with this disclosure, which may contain any of the aforementioned devices. An etch stop 215 is disposed on underlying layer 205, which may be comprised of silicon nitride (Si₃N₄), silicon carbide (SiC), or any other etch resistant material.

[0021] **Figure 3** illustrates a zeolite film 310 disposed on underlying layer 205 after a zeolite – solvent solution, such as zeolite – solvent solution 115 as shown in

Figure 1, has been deposited on underlying layer 205 and at least some of the solvent has been removed in step 305. Step 305 may include deposition of a zeolite – solvent solution. Deposition of a zeolite – solvent solution may include any variety of known methods for deposition of materials in semiconductor fabrication. For example, the zeolite – solvent solution may be deposited by dip-coating underlying layer 205 in the zeolite – solvent solution. As another example, the zeolite – solvent solution may be deposited by spin-coating the zeolite – solvent solution on underlying layer 205. It is readily apparent that these well-known methods, as well as other well-known methods, of depositing dielectric material may be used to deposit the solvent solution on underlying layer 205.

[0022] Furthermore, step 305 may include removing at least some of the solvent from the zeolite – solvent solution to form zeolite film 310. Removing at least some of the solvent may include drying the zeolite – solvent solution to remove at least some of the solvent. For example, drying may be done in air or by vacuum.

[0023] **Figure 4** illustrates zeolite - carbon doped oxide (CDO) composite film 415 disposed on underlying layer 205, after a CDO has been deposited in a zeolite film, such as zeolite film 310 shown in **Figure 3**, in step 405. As an example CDO 410 may be silicon oxide, ($\text{SiC}_x\text{O}_y\text{H}_z$), or any other CDO. Step 405 may be any process where CDO 410 is deposited in a zeolite film. As an illustrative example of CDO deposition process 405, CDO 410 may be deposited in a zeolite film by chemical vapor deposition.

[0024] As shown in **Figure 5**, after CDO 410 is deposited, the zeolite – CDO may be re-flowed and calcinated, such as in calcinations process 505. Calcination process 505 may form a zeolite – CDO composite dielectric/film, such as zeolite – CDO composite

dilectric layer 510. Step 505 may be any process where the zeolite – CDO composite film 415, as shown in **Figure 4**, is heated and cooled to form zeolite – CDO composite dielectric layer 510, shown if **Figure 5**.

[0025] For example, calcination process 505 may include heating zeolite – CDO composite film 415. As a specific example, zeolite – CDO composite film 415 may be heated at an ambient temperature in the range of 300°C to 550°C for an amount of time. Heating may be done in oven, furnace, or any other device for heating interconnect structures. Heating may also cause the CDO components of zeolite – CDO composite film 415 to reflow and form a continuous matrix. Calcination process 505 may also include oxidizing zeolite – CDO composite film 415. Oxidizing zeolite – CDO composite film 415 may include allowing the air to oxidize zeolite – CDO composite film 415 over a period of time or exposing the structure to an induced ozone. Moreover, calcination process 505 may also include vacuuming to remove any side-product from zeolite – CDO composite film 415.

[0026] It is readily apparent that each of the methods of removing liquid from zeolite – CDO composite film 415 may individually or combinationally be used to extract at least some liquid from zeolite – CDO composite film 415. As an illustrative example, zeolite – CDO composite film 415 may be heated in an oven while under a vacuum. Calcination process 505 may also include cooling zeolite – CDO composite film 415, after heating, to form layer 510 and freeze layer 510 into a solid form. Cooling may include allowing layer 510 to cool at room temperature for an amount of time at a variable cooling rate. Cooling may also include refrigeration within a refrigerator or other cooling device to cool layer 510.

[0027] As shown in **Figure 6** and **Figure 7**, further damascene processing may be done on the zeolite – CDO composite dielectric layer 510. In **Figure 6**, a via opening 605 and a trench 610 is etched in zeolite – CDO composite dielectric layer 510. In **Figure 7**, a barrier layer 705 is deposited on the surfaces of zeolite – CDO composite dielectric layer 510. Then conductive material 710 is formed in via opening 605 and trench 610. It is apparent that other well-known steps, such as chemical mechanical polish (CMP) and materials, such as copper, tantalum, etc., in the damascene process have been left out so as not to obscure the discussion of zeolite – CDO composite material.

[0028] Therefore, as discussed above a composite zeolite – CDO dielectric layer/film may be created that has the low k dielectric constant and is able to form a uniform layer. The composite zeolite – CDO dielectric may have greater mechanical strength than a CDO film, because of the addition of zeolite. Furthermore, instead of the non-uniform film that is usually created with pure zeolite films, a uniform film may be created with the introduction of a CDO material into the composite.

[0029] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.